AMENDMENTS TO THE CLAIMS

1-8. (Canceled).

9. (Currently Amended) A data sharing apparatus comprising:

a data bus having a data width;

a memory;

a first-endian processor logically connected to said memory in a first-endian byte order via said data bus;

a second-endian processor logically connected to said memory in the first-endian byte order via said data bus; and

an address conversion unit operable: ~~to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second-endian processor performs a memory access for data having a smaller width than the width of the data bus, and operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus;~~

(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data;

(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data; and

(iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus,

wherein said~~the~~ memory stores structure data to be accessed by ~~the~~ said first-endian processor and ~~the~~ said second-endian processor,

~~the~~ said first-endian processor executes a first program that defines the structure data, ~~and~~

saidthe second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, ~~said~~ the data being defined in an order within the basic word length, and ~~said~~ the order being in reverse to an order in the first program, and

said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor.

10. (Previously Presented) The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

11. (Previously Presented) The data sharing apparatus according to Claim 10,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

12-15. (Canceled).

16. (Currently Amended) A data sharing apparatus comprising:

a data bus having a data width;

a memory;

a first-endian processor logically connected to said memory in a first-endian byte order via said data bus;

a second-endian processor logically connected to said memory in the first-endian byte order

via said data bus; and

an address conversion unit operable: ~~to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second-endian processor performs a memory access for data having a smaller width than the width of the data bus, and operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus;~~

(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data;

(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data; and

(iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus,

a cache memory logically connected to the data bus in a second-endian byte order

wherein ~~the~~ said memory stores structure data to be accessed by ~~the~~ said first-endian processor and ~~the~~ said second-endian processor,

~~the~~ said first-endian processor executes a first program that defines the structure data, and

~~the~~ said second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program, and

said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor.

17. (Previously Presented) The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

18. (Previously Presented) The data sharing apparatus according to Claim 17,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

19. (Currently Amended) A method of sharing data in a data processing apparatus which includes a first-endian type processor and a second-endian type processor, and a memory to which both processors are connected via a data bus in a first-endian byte order, the method comprising:

causing the first processor to execute a program that defines structure data, causing the second processor to execute a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared in the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data for the first-endian type processor, causing the first-endian processor to read or write the structure data to communicate with the second-endian processor, and causing the second-endian processor to read or write the structure data to communicate with the first-endian processor;~~;~~ ~~and~~

~~performing an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, in the case where the second-endian processor performs a memory access for data with a smaller width than the width of the data bus, and not performing the address conversion in the case where the second-endian processor performs a memory access for data having the width of the data bus~~

(i) inverting values of two least significant bits of an address outputted from the second-

endian processor and outputting an address including the inverted values to the memory when the second-endian processor performs a memory access for 8-bit data;

(ii) inverting a value of a second least significant bit of an address outputted from the second-endian processor and outputting an address including the inverted value to the memory when the second-endian processor performs a memory access for 16-bit data; and

(iii) outputting an address from the second-endian processor to the memory without address conversion when the second-endian processor performs a memory access for data having the width of the first data bus.

20-23. (Canceled).

24. (Previously Presented) The data sharing apparatus according to claim 16, wherein the first-endian type is big-endian and the second-endian type is little-endian.

25. (Previously Presented) The data sharing apparatus according to claim 16, wherein the first-endian type is little-endian and the second-endian type is big-endian.

26. (Previously Presented) The method according to claim 19, wherein the first-endian type is big-endian and the second-endian type is little-endian.

27. (Previously Presented) The method according to claim 19, wherein the first-endian type is little-endian and the second-endian type is big-endian.

28. (New) A data sharing apparatus comprising:

a first-endian processor operable to execute a first program in which a first structure data is defined;

a first-endian type memory operable to store shared data;

a first address bus logically connected to said first-endian processor and said first-endian type

memory;

a first data bus logically connected to said first-endian processor and said first-endian type memory;

a second-endian processor operable to execute a second program in which a second structure data is defined and to communicate with said first-endian processor via the shared data stored in said first-endian type memory,

a second address bus which is logically connected to said second-endian processor;

a second data bus logically connected to said second-endian processor, said second data bus being logically connected to the first data bus in a first-endian order; and

an address conversion unit, logically connected to said first address bus and said second address bus, operable:

(i) to invert values of two least significant bits of an address in said second address bus and output an address including the inverted values to said first address bus when said second-endian processor performs a memory access for 8-bit data;

(ii) to invert a value of a second least significant bit of an address in said second address bus and output an address including the inverted value to said first address bus when said second-endian processor performs a memory access for 16-bit data; and

(iii) to output an address from said second address bus to said first address bus without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus,

wherein the shared data is defined as the first structure data in said first-endian processor and is defined as the second structure data in said second-endian processor,

the first structure data and the second structure data include data that is smaller than a basic word length,

the data being defined in an order within the basic word length,

the order in a definition of the first structure data being in reverse to an order in a definition of the second structure data, and

said first-endian processor reads or writes the shared data to communicate with said second-

endian processor and said second-endian processor reads or writes the shared data to communicate with said first-endian processor.

29. (New) A pre-processing method which performs pre-processing prior to compiling a first and a second source program, said method comprising:

receiving the first source program for a first-endian processor and the second source program for a second-endian processor;

detecting structure data to be shared by the first-endian processor and the second-endian processor; and

switching an order of variables in the detected structure data so that an order of variables within a basic word length for the second source program is in reverse to an order of variables within a basic word length for the first source program.

30. (New) The pre processing method according to claim 29, further, comprising

inserting dummy data into an 8-bit blank within the basic word length in the detected structure data of the first source program and the second source program, so that an order of a dummy byte and the variables within the basic word length for the second source program is in reverse to an order of a dummy byte and the variables within the basic word length for the first source program.

31. (New) A pre-processing apparatus which performs pre-processing prior to compiling a first and a second source program comprising:

a receiving unit operable to receive the first source program for a first-endian processor and the second source program for a second-endian processor;

a detecting unit operable to detect structure data to be shared by the first-endian processor and the second-endian processor; and

a switching unit operable to switch an order of variables in the detected structure data so that an order of variables within a basic word length for the second source program is in reverse to an

order of variables within a basic word length of the first source program.